LDO with low voltage bandgap

Features

- 2.8V-5.5V input voltage low dropout regulator
- Output voltage of 1.8V +/- 60mV
- VDD detection circuit with separated power on reset output
- internal low voltage cascade bandgap
- Pure 150 nm CMOS technology, core cell area: 0.066mm² LDO
- 0.024mm^2 Bandgap without internal stabilizing capacitors
- Operating temperature range:
  –40 – +125 °C

General Description

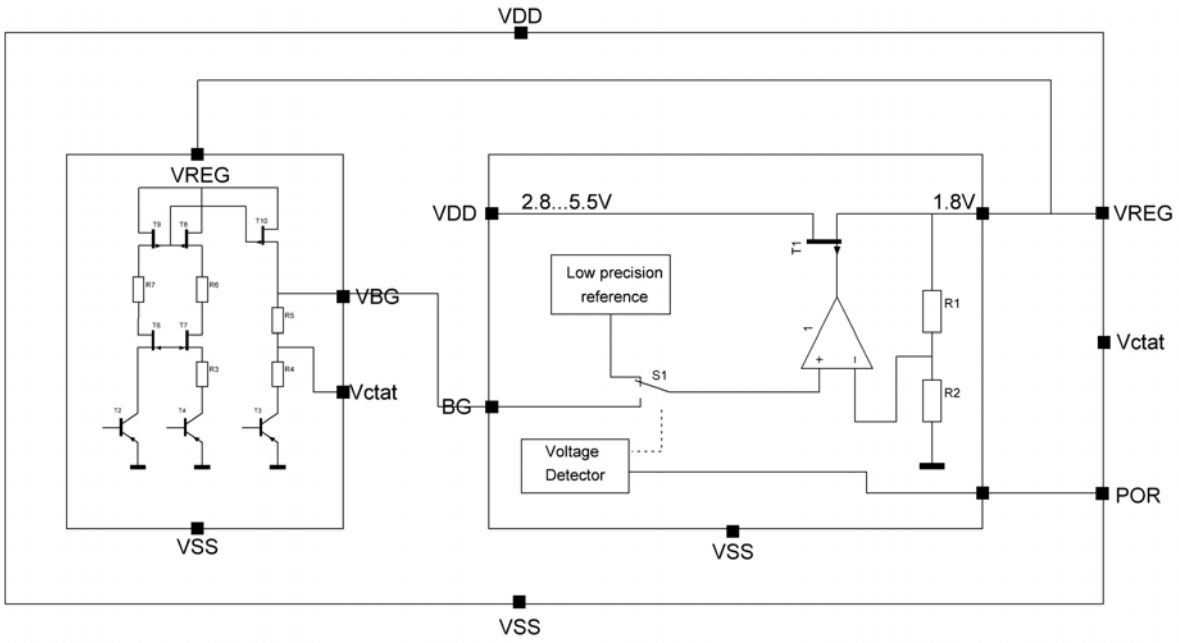
IMST's low dropout voltage regulator solution provides an output voltage of 1.8V over and input supply voltage range of 2.8V up to 5.5V @ a maximum output current of 8mA.

The internal bandgap block provides a constant bandgap voltage for the LDO.

An internal voltage detector detects the input voltage and switches on the power on reset signal (POR) which can be used to reset e.g. a digital block. The second internal detector switches between the non precision and bandgap reference after a defined time (around 50us).

During this time period the bandgap circuit can be start up and generates a stabilize bandgap voltage.

Block diagram



ELECTRICAL CHARACTERISTICS

Operating Conditions, Vcc = +2.8 – 5.5 V, T_A = -40 to +125°C, Typical values are taken at Vcc = 3V, T_A = +27°C, (unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	UNIT
Input Voltage Range		2.8	3.0	5.5	V
Ouput voltage Range		1.74	1.8	1.86	V
Output Current				8.0	mA
Bandgap Voltage		1.133	1.16	1.184	V
Current without load		1.1		1.9	mA
Output Cap on chip			20.0		pF
Process	150nm CMOS				
Status	In Fab				